Why optical lithography will live forever

Timothy A. Brunner[a]
IBM SRDC, 2070 Route 52, Hopewell Junction, New York 12533

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A lithographic process capable of manufacturing state of the art chips faces many difficult challenges. Not only must the process resolve the minimum feature size but overlay errors must be held to tight tolerances, exquisitely complex patterns must be printed with high yield, and the overall cost of the process must be acceptable. Achieving acceptable chip cost using an expensive exposure tool is strongly linked to high throughput, and this in turn is linked to resist processes with high sensitivity. In recent years, chemically amplified resist processes have dominated state-of-the-art production because of their high resolution and excellent sensitivity. This article will consider limitations of resolution for production lithography, both the resolution limits of the exposure tool itself and the resolution limits of the resist process. Among the most important considerations for production processes is the tradeoff between resist process sensitivity and resolution. Fundamental reasons underlying the success of optical lithography for manufacturing integrated circuits will be described. These considerations will illuminate the challenges and opportunities for future lithographic methods. © *2003 American Vacuum Society.* [DOI: 10.1116/1.1619954]

I. INTRODUCTION

Over the years many lithographic patterning methods have been devised. Almost every type of exposure energy—photons of various wavelength or particle beams—has been combined with innovative contact, proximity, or projection methods. There are myriad applications for such patterning in the research, development, and manufacture of electronic, photonic, and optical devices. This article will focus on trends in the lithographic processes used for the high volume manufacture of integrated circuits.

The requirements of such processes are quite well known by chip manufacturers around the world, and include:

1. working resolution, with adequate linewidth control in the presence of unavoidable exposure and focus variations;
2. overlay capability, including the ability to compensate for wafer size changes due to processing;
3. high fidelity, such that complex chip patterns are printed without defects; and
4. economic considerations, especially high throughput, e.g., 100 wafers/h.

Chip manufacturing has shown steady improvements in a variety of metrics over the past 3 decades. Many of these metrics show exponential dependence[1,2] and are usually thought of as forms of Moore's law. Figure 1 shows one of the most important such plots, where cost per function—both dynamic random access memory (DRAM) bits and logic gates—are observed to decrease exponentially by roughly 33% per year. While not scientifically fundamental, it is this cost metric which drives the integrated circuit industry forward, and has driven the steady progress of lithography.

The lithographic process can be thought of as a flow of information, as illustrated in Fig. 2, beginning with the pattern design in the form of a mask data file and ending up as a physically patterned device layer. Each step in the lithographic process holds the possibility of losing information, thereby degrading the desired pattern. This article will focus on two major parts of the process: the projection of the pattern energy profile and the resist process. Section II will discuss the resolution limits of production exposure tools, i.e., the resolution of the aerial image profile. The Rayleigh equation will guide this discussion focusing on the key parameters of exposure wavelength λ, projector numerical aperture (NA), and k_1. Emerging design paradigms which maximize the patterning fidelity at low k_1 will be discussed. Multiple exposure methods will be mentioned as a way of breaking the $k_1=0.25$ half-pitch barrier. Section III will consider the resolution limits of resist processes, with emphasis on high throughput chemically amplified resist processes. Resist blurring, pattern collapse, and shot noise issues will be discussed. Finally, Sec. IV will speculate on future opportunities for optical lithography, beginning with an accounting of the fundamental strengths of optical lithography.

II. PRODUCTION EXPOSURE TOOL RESOLUTION

The fundamental limit of the resolution of an optical projection exposure tool is captured by the well-known Rayleigh scaling equation[3]

$$W_{\min}=k_1\times\frac{\lambda}{\mathrm{NA}}, \tag{1}$$

where $W_{\min}$ is the minimum linewidth of the printed feature, λ is the exposure wavelength, NA is the numerical aperture of the projection optics, and k_1 is a dimensionless scaling parameter. Let us now consider the progress in each of the three factors which define the projector resolution.

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[a] Electronic mail: tbrunner@us.ibm.com

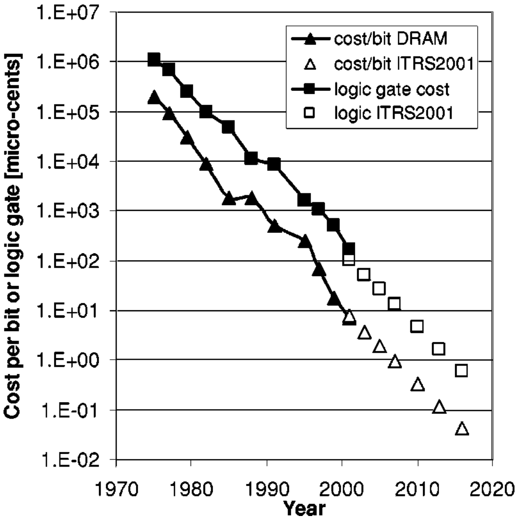

FIG. 1. History of cost per DRAM bit and cost per CMOS logic gate, along with roadmap projections. This is Moore's law which powers the progress of production lithography.

A. Exposure wavelength

There is a strong motivation to shrink wavelength since minimum linewidth scales proportionally. Table I lists several standard lithographic wavelengths. The fraction $\Delta\lambda/\lambda_{\mathrm{prev}}$ represents the relative improvement in moving from a previous wavelength λ_{prev} to the next generation wavelength $\lambda=\lambda_{\mathrm{prev}}-\Delta\lambda$. For example, the 32% drop in wavelength from *I* line to KrF lithography was a huge driving force, equivalent to roughly one integrated circuit generation shrink all by itself. The invention of chemically amplified resist systems[4] was a key enabling technology for KrF manufacturing, and is firmly established in all advanced lithography production. Over the past 1–2 yr, ArF lithography has begun to ramp up in production, with a 22% resolution improvement over KrF. Roughly 10 yr of intense research and development—particularly in the areas of resist processes, system contamination and optical degradation—were needed to enable 193 nm production.

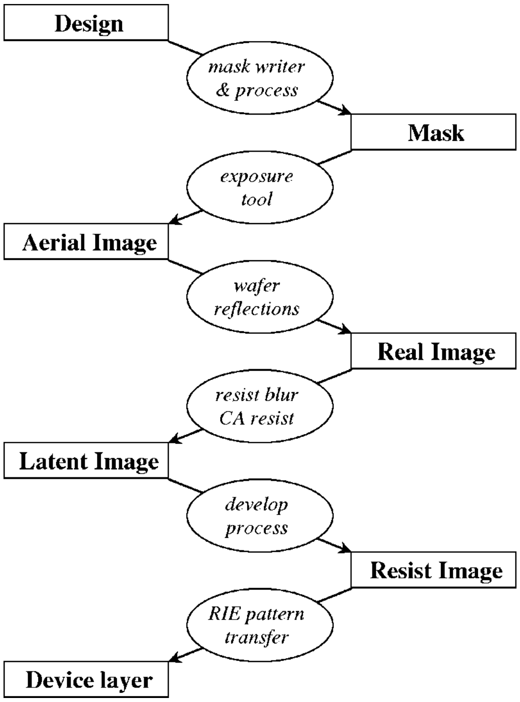

FIG. 2. Information flow in the lithographic process. Every step is an opportunity to lose information or distort the desired pattern.

TABLE I. Wavelengths for optical lithography. Resolution W_{min} uses $k_1=0.3$ and DOF uses $k_3=1$, assuming NA=0.9 for all wavelengths except EUV, which assumed NA=0.25.

	λ (nm)	$\Delta\lambda/\lambda_{\mathrm{prev}}$ (%)	W_{min} (nm)	DOF (nm)
G line Hg	436	⋯	145	386
I line Hg	365	16	122	324
KrF	248.3	32	83	220
ArF	193.4	22	64	171
F_2	157.6	19	53	140
EUV	13.5	91	16	213

The F_2 laser, operating at roughly 158 nm, offers another significant incremental 19% advance relative to ArF. Over the past 5 yr, fundamental advances have been made in many aspects of F_2 lithography, especially the development of a dimensionally stable fluorinated silica mask material, high NA optical designs which compensate for the intrinsic birefringence of calcium fluoride, and prototype fluorinated polymer resist materials. But significant technical challenges remain, most notably the production of CaF_2 "blanks" of suitable size and quality for building lens elements. It is not yet clear when overall F_2 lithographic capability will exceed ArF lithography.

Extreme ultraviolet (EUV) lithography offers a revolutionary advance in exposure tool imagery, with a spectacular 91% wavelength reduction over F_2 lithography. In order to make resolution comparisons, Table I also plots the W_{min} resolution for each wavelength, assuming $k_1=0.3$ and a very high NA of 0.9, except for EUV which assumes a more achievable NA=0.25. Even at the smaller NA, the resolving capability of an EUV projector offers better than threefold improvement over F_2. Many challenges must be overcome in order to use EUV lithography for chip production, especially tool throughput and other economic challenges. The tool throughput issue has two intertwined aspects: a sufficiently bright source coupled with a sufficiently sensitive resist process. At the present time, only very simple circuit patterns with a few ring oscillator gates have been printed with EUV lithography.

B. Numerical aperture

Full field optical exposure tools with NA>0.8 are currently in use for chip production. High NA optical systems must always face the problem of limited depth of focus (DOF). The Rayleigh scaling of DOF, modified for validity at high NA,[5,6] is given by

$$\mathrm{DOF}=k_3\times\frac{\lambda}{4\sin^2(\theta/2)}=k_3\times\frac{\lambda}{2(1-\sqrt{1-\mathrm{NA}^2})},\qquad(2)$$

where $\theta=\sin^{-1}(\mathrm{NA})$ is the maximum oblique wave angle and k_3 is a dimensionless factor of order unity which depends on the imaging details. The DOF decreases with increasing NA even more steeply than the traditional paraxial NA^{-2} Rayleigh scaling.[3] The progress of increasing NA optics over the years has been driven by two aspects. One aspect is the increasing skill of lens designers and lens builders in realizing high NA optics with very low aberration levels. The other aspect is the continued improvement in the chip building process, with progress in all aspects of process focus control including wafer flatness, autofocus/autoleveling systems, thinner resist processes, and decreased process topography via advanced methods such as chemical mechanical polishing.

Further increases in NA are motivated by the difficulties of changing exposure wavelength. Air projectors with NA ≈ 0.9 are likely in the near future, and immersion lithography with $\mathrm{NA}>1$ is undergoing intense research.[7] In addition to the difficulties of the very low DOF, new issues arise with such high NA. Polarization plays a fundamental role as the angle of incidence approaches or exceeds Brewster's angle. The transverse magnetic (TM) polarization component will have reduced image contrast due to vector effects,[6] and this will reduce the exposure latitude. The oblique propagation angle within the resist controls this effect, so resist materials with larger index of refraction would improve the situation. Manipulation of the illumination polarization is another possibility. Other unusual thin film interference and swing curve effects[8] are caused by the highly oblique waves. For good process control, a capable super-high NA resist process will need a thin imaging layer to conserve DOF, an excellent bottom antireflective coat layer to control swing curve effects, and possibly a top antireflective coat layer to improve the coupling of high angle radiation into the resist.[6]

Immersion lithography is a radical approach to increasing the effective NA. While the fundamental principles have long been known, and are used every day in biological microscopy, it is only recently that the method is being seriously examined for production lithography.[7] For 193 nm lithography, purified water is a suitable immersion fluid with $n\approx 1.44$. There are a number of open issues with regard to chip production with immersion lithography including:

(1) moderate to severe loss of image contrast for the TM polarization;
(2) fast, clean fluid dispensing onto wafer;
(3) bubble formation and other optical distortion during wafer scanning;
(4) resist process interactions with fluid; and
(5) lens contamination issues.

It is too early to tell whether immersion lithography will play a significant role in future chip production.

C. k_1 scaling factor

For line gratings, diffraction considerations dictate a minimum pitch limit of 0.5 λ/NA, which is the same as a $k_1 \geqslant 0.25$ limit for grating half pitch. Many state of the art manufacturing processes produce complementary metal–oxide–semiconductor (CMOS) gate geometries with $k_1 < 0.25$, and this is possible because the spacing between gates is larger than the gate linewidth. The k_1 factor is a useful measure of the degree of difficulty of printing a particular feature. When $k_1 > 0.6$, the lithographic process is relatively easy and tolerant of process deviations. As k_1 shrinks, the imaging process becomes increasingly difficult with small process deviations causing unacceptably large pattern changes. Tremendous progress has been made in recent years to reduce k_1 through the use of resolution enhancement technology (RET) such as various phase shift mask approaches, off-axis illumination, subresolution assist features, optical proximity correction methods, and many other approaches. Many RET methods are superb at printing grating test patterns, but become problematic when used with actual circuit patterns. The fundamental reason for this is that near the $k_1=0.25$ half-pitch limit, the images are formed from just two diffraction orders which interfere to form a sinusoidal periodic grating image. Recently, an interesting design philosophy[9] has emerged, in which the critical pattern levels are designed to resemble periodic gratings. The great virtue of this approach is that advanced RET methods can be applied in a straightforward manner to print these patterns at high density.

A number of research thrusts have sought to break through the $k_1=0.25$ half-pitch barrier. Direct optical approaches include two photon lithography[10] or the use of entangled photons,[11] but the capability to print patterns as complex as chip designs has not been demonstrated. Another class of approaches doubles the spatial frequency by printing each edge in the image as a line, including sidewall lithography,[12] where a deposition step controls the linewidth and hybrid lithography[13] which makes use of a unique resist process with both positive and negative tone characteristics. These frequency doubling processes suffer from profile asymmetries as well as design complications similar to those of phase edge lithography. Another class of approaches is to use multiple exposures. Unfortunately, in a normal resist process where the intensity images of multiple exposures would simply add, it is not possible to break the $k_1=0.25$ half-pitch limit. Through use of a multiple expose/multiple etch method, it is possible to increase the spatial frequency beyond the normal limit. In one such scheme,[14] a sacrificial thin film layer is used to accumulate the total image pattern. The major virtue of the multiple expose/multiple etch approach is that it can be practiced with current equipment and processes. Along with obvious cost issues, overlay errors and linewidth differences between the two exposures must be tightly controlled to produce acceptable patterns.

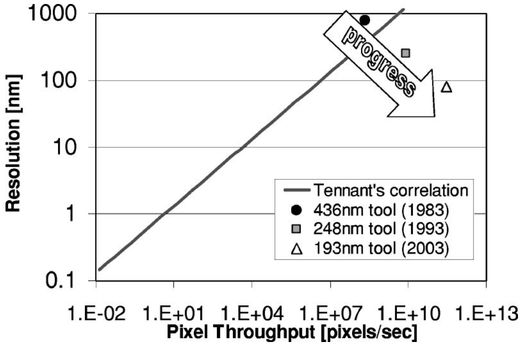

FIG. 3. Correlation of lithographic resolution and pixel throughput. The solid line represents the correlation noted by Tennant in Ref. 13, and represented by the equation $P \approx 4.3\,R^3$, where R is the resolution in nm and P is the throughput in pixels per second. The three isolated points represent production optical lithography tools, and illustrate the progress in both resolution and throughput.

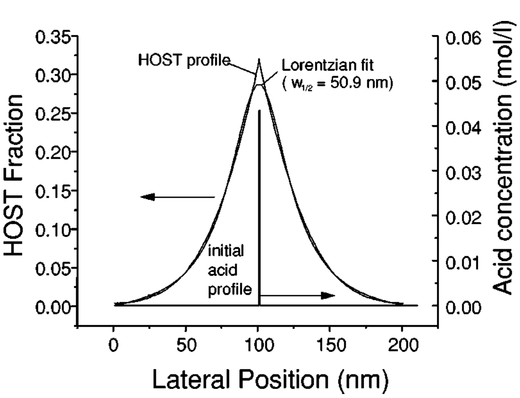

FIG. 4. Resist blur function calculated for an ESCAP-type chemically amplified resist process. The initial acid profile was assumed to the 1 nm wide but the PEB reaction diffusion creates a reacted polymer profile with FWHM of roughly 50 nm, similar to that of direct experimental measurement of the blur function.

III. PRODUCTION RESIST PROCESS RESOLUTION

Section II has described exposure tools and imaging methods which are capable of producing high resolution aerial image profiles with the desired pattern information, but this must somehow be accurately converted into a physical pattern on the wafer. Processes with very high resolution can be very slow. Tennant has characterized this resolution/throughput tradeoff[15] over a wide range of lithographic methods. His correlation, modified from area throughput to pixel throughput, is plotted as the solid line in Fig. 3. For comparison, resolution and throughput data points are plotted for three eras of optical lithography production tools.

The highest resolution imaging methods use the energy profile to directly drive chemistry on the substrate. For example, patterns with several nm resolution have been written with e-beam inorganic resists[16] or self-assembled monolayer resists,[17] although at very high doses on the order of 1 C/cm^2 (i.e., in more usual units, $10^6\,\mu\text{C/cm}^2$). Poly(methylmethacrylate) (PMMA) has been able to resolve 15 nm dense line gratings with e-beam exposure. Unfortunately, the dose requirements of such nonamplified resists are orders of magnitude higher than those needed for production lithography. Virtually all leading edge chip production resist processes are chemically amplified, driven by the requirements of high throughput lithography. The following subsections will discuss several key aspects of production resist processes which can limit resolution.

A. Resist blur in chemically amplified resists

The chemically amplified resist process uses the energy profile created by the exposure tool to drive the creation of a catalyst profile within the resist film. A subsequent postexposure bake (PEB) is used to drive the main solubility-changing polymer reaction which is catalytically enhanced. One quantum of energy absorption creates one molecule of catalyst which can drive hundreds of solubility-changing reactions, hence the marvelous sensitivity of chemically amplified resists. But a rigorous, quantitative description of the simultaneous chemical reaction and diffusion transport during the PEB shows that the solubility-changing reaction of the catalyst is not entirely local, but rather spreads out spatially. Figure 4 shows the one-dimensional blur function for a typical deep ultraviolet chemically amplified resist calculated by such a rigorous method.[18] The blur function resembles a Lorentzian line shape with a full width half maximum (FWHM) of 51 nm. Recently, a direct experimental probe[19] applied a modulation transfer function (MTF) approach, in combination with interferometric lithography, to measure the resist point spread function (PSF). A good match[16] was found between the measured PSF blur function and the calculated resist blur function of Fig. 4. While resist blur functions have been known and used for many years,[20] the MTF experiment and reaction–diffusion calculation of Fig. 4 have provided the most direct measurement and deepest understanding of this important phenomenon.

Obviously, the resist blur function constitutes a resolution-limiting aspect of production lithography; an energy profile with resolution of 15 nm would be wasted in a resist process with 50 nm blur function. But this 50 nm blur is not fundamental, and can be improved upon. One approach is to trade off resist sensitivity for resolution, by reducing the catalytic amplification factor. Unfortunately, the economics of production are very demanding of resist sensitivity. This is particularly true of EUV lithography, where dim sources and losses in the optics create an extreme need for resist sensitivity.

B. Resist collapse

As dimensions continue to shrink, resist collapse has become a much more important problem with state of the art production processes. (It is disheartening to the lithographer to see a perfectly formed high resolution resist line of the proper dimension lying askew on the wafer surface.) The root cause of collapse[21] is driven by surface tension effects during the drying after wet development. Recent work at the University of Wisconsin[22] has shown that the attainable as-

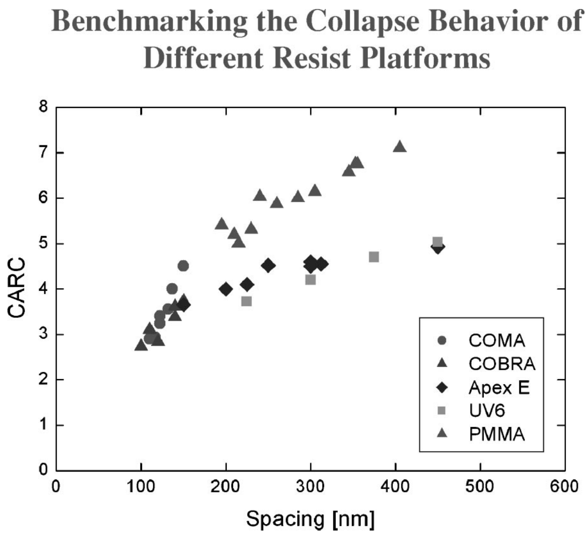

FIG. 5. Collapse behavior of various resist platforms. The critical aspect ratio for collapse (CARC) is defined to be the ratio of the resist thickness to the linewidth where collapse would begin. CARC was found to decrease for smaller feature sizes for all resist platforms studied by Cao *et al.* at the University of Wisconsin (Ref. 19).

pect ratio is decreasing with feature size. This unfavorable scaling has been observed in a number of resist polymer platforms, as shown in Fig. 5.

Several strategies are being explored to avoid collapse. The most obvious approach is to use a thinner resist film, which usually results in complications of the etch process and the level integration scheme. Another approach is to reduce the surface tension during development drying by use of surfactants or solvents. The most powerful approach is to reduce surface tension to zero by use of a triple-point CO_2 rinse,[23] but this is currently not production worthy.

C. Shot noise and quantum statistical effects

We tend to think of exposure energy profiles as smooth, continuous functions as assumed by most of our simulation models. In fact, as features continue to shrink we are increasingly entering a quantum realm. The true exposure energy profile is a discrete collection of energy quanta with random fluctuations, and the latent image inside the chemically amplified resist is a finite collection of catalyst molecules. Just like the classic example of a photomultiplier tube, the statistical fluctuations are dominated by the relatively small number of quanta before amplification. The statistical variations are a fundamental form of noise in the flow of pattern information, and are observed as line edge roughness and random feature variations.

The amount of quantum noise is fundamentally tied to the number of quanta per resolvable element. An insensitive resist, like PMMA, requires huge numbers of quanta to expose, and quantum fluctuations are relatively unimportant. On the other hand, a sensitive chemically amplified resist works with fewer quanta, hence more fluctuation. The resist blur function defines a natural resolution area within which to count quanta. Table II collects some quantum noise data for several types of lithography where a 50 nm square pixel was chosen to crudely approximate a typical chemical amplified resist blur. The number of quanta falling within the pixel is used to calculate a 3σ dose variation. 193 nm lithography has a large number of quanta within each pixel and the statistical fluctuations are expected to be small. EUV lithography has a smaller number of quanta exposing a sensitive 1 mJ/cm^2 resist, and statistical fluctuations are larger than at 193 nm. The 50 kV e beam and 100 kV ion beam face significant quantum noise issues when used with sensitive chemically amplified resists. The statistical fluctuation problems become worse as pattern resolution improves and as the resist dose goes down, both nominally desirable trends for production lithography. For example, if we choose a 25 nm lithographic pixel, the fluctuations increase by a factor of 4 relative to the 50 nm pixel. The brief discussion herein has been qualitative and oversimplified. Recent quantum noise work takes into account the quantum statistics of the chemical amplified resist process,[24] and should provide a better basis for understanding the tradeoff of resolution and sensitivity for chemically amplified resists.

IV. FUTURE OPPORTUNITIES FOR OPTICAL LITHOGRAPHY

We begin this section with a review of the fundamental strengths of 193 nm optical lithography for chip production. Through the use of high NA optics and sophisticated imaging methods, sufficient resolution to support ground rules for 65 nm node designs has been achieved. It is notable that this level of resolution is being achieved at high throughputs, on the order of 100 300 mm wafers/h. Chemically amplified resist systems have been developed with the required combination of resolution and sensitivity. Many 193 nm quanta are used to form the image, so shot noise effects are relatively low. Precision, high-speed stages enable an overall

TABLE II. Quantum fluctuations of number of quanta in 50 nm square pixel for various lithographic approaches.

Lithography	Energy (eV)	Resist dose (mJ/cm^2)	No. quanta 50 nm pixel	3σ dose variation (%)
193 nm	6.4	20	500 000	0.4
EUV—13.5 nm	92	2	3400	5
X ray—1.3 nm	920	40	6800	4
e beam	50 000	150 (3 $\mu C/cm^2$)	470	14
Ion beam	100 000	50 (0.5 $\mu C/cm^2$)	78	34

overlay error control capability which can support the 65 nm node at the required wafer throughput. The high throughput levels are a key aspect to the overall cost effectiveness of 193 nm lithography. An established mask infrastructure is able to supply photomasks of the necessary quality. Extremely complex pattern layers can be printed with very low defect levels, and mask pellicles are able to prevent particulate mask defects. On a more general level, the technology has reached a high level of maturity and sophistication due to decades of research, development, and manufacturing learning.

Future lithographic production methods must follow the prime directive of reduced cost per function shown in Fig. 1. While aerial image profiles of next generation lithography (NGL) candidates possess higher resolution than 193 nm aerial image profiles, it is not at all clear that this potential resolution advantage can be captured at the needed throughput levels. Resist blur of chemically amplified resists may be a limiting factor, particularly at high throughput when high amplification is needed. The fewer quanta of most NGL methods raise concerns about quantum noise, again made worse at highest throughput. Resist collapse issues are not improved by use of a different exposure energy. The rapid improvements in the resolution of high throughput production lithography enjoyed over the past 40 yr currently face formidable barriers, and are likely to slow. This does not mean that lithographic innovation will cease. Future opportunities in lithography lie in directions other than ‘‘mindless shrinking.’’

One area of opportunity aims to address the growing cost of a mask set. Such large nonrecurring engineering expenses can dominate the cost of designs where there are few wafers produced, e.g., prototype designs, customized chips, etc. The fundamental advantages of optical lithography can be brought to bear on this problem. A programmable micromirror array can generate patterns for an advanced optical mask writer or an optical maskless lithography tool.[25] The realization of such tools face nontrivial challenges, including the fabrication of micromirror arrays of sufficient capability, rapid transfer of huge amounts of pattern data, and dataprep methods. But the formidable infrastructure of 193 nm lithography processes can be utilized immediately, and the approach could extend into F_2 and EUV sources.

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